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EXAMINER	
CRAWFORD, LATANYA N	

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/557,746	SHIBATA, SATOSHI	
	Examiner	Art Unit	
	LATANYA CRAWFORD	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-4 and 8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7,9-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the correspondence filed on 03/10/2009. Currently, claims 5-7, 9-17 and newly added claims 18-25 are pending. Claims 1-4, & 8 have been cancelled.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the gate electrode that is formed on the semiconductor region is non-uniformly distributed" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because region 104 (pn junction at a third depth) of Fig. 1(d) is shaded and has the same shape as the gate insulator 106 depicted in 2(a). The illustrations are confusing and are not shown distinct from one another.

Refer to § 1.84 Standards for drawings:

(m) Shading . The use of shading in views is encouraged if it aids in understanding the invention and if it does not reduce legibility. Shading is used to indicate the surface or shape of spherical, cylindrical, and conical elements of an object. Flat parts may also be lightly shaded. Such shading is preferred in the case of parts shown in perspective, but not for cross sections. See paragraph (h)(3) of this section. Spaced lines for shading are preferred. These lines must be thin, as few in number as practicable, and they must contrast with the rest of the drawings. As a substitute for shading, heavy lines on the shade side of objects can be used except where they superimpose on each other or obscure reference characters. Light should come from the upper left corner at an angle of 45°. Surface delineations should preferably be shown by proper shading. Solid black shading areas are not permitted, except when used to represent bar graphs or color.

Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings.

The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 5, 7 & 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by En (US Patent 6,548,361 B1).

Regarding claim 5, En et al. discloses a method for manufacturing a semiconductor device, comprising the steps of: forming an amorphous layer (64) in a region from a surface of a semiconductor region of a first conductivity type to a first depth (column 5, lines 30-35;column 6, lines 25-50) fig. 3b ; by heat treating the amorphous layer at a prescribed temperature (column 7, lines 56-67;column 8, lines 1-4), restoring a crystal structure of the amorphous layer in a region from the first depth (40) to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth; after the heat treating, forming a first impurity layer of a second conductivity type which has a pn junction (28) at a third depth that is shallower than the second depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth (column 7, lines 15-23) ; and restoring a crystal structure of the amorphous layer in a region from the surface of the

semiconductor region to the second depth using solid phase epitaxy (column 8, lines 1-4).

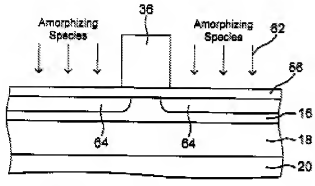

FIG. 3B

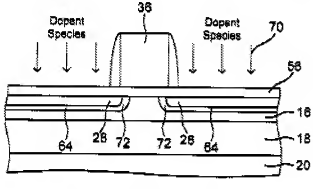

FIG. 3C

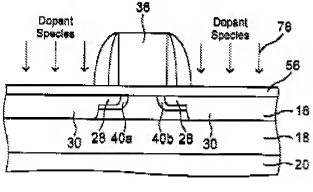

FIG. 3D

Regarding claim 7, En et al. discloses wherein the prescribed temperature is in a in a range of 475°C to 600°C (column 7, lines 56-67).

Regarding claim 18, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C (column 7, lines 56-67; column 8, lines 1-4).

Regarding claim 19, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 700 °C (column 7, lines 56-67; column 8, lines 1-4).

Regarding claim 20, En et al. discloses wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy (column 8, lines 1-4).

6. Claims 13, 16, 24, & 25 are rejected under 35 U.S.C. 102(b) as being anticipated by En (US Patent 6,548,361 B1).

Regarding claim 13, En et al. discloses a method for manufacturing a semiconductor device, comprising the steps of: forming a gate electrode (36) on a semiconductor region of a first conductivity type with a gate insulating film (38/56) interposed there between (column 5, lines 30-35;column 6, lines 14-24), forming an amorphous layer (64) in a region from a surface of the semiconductor region to a first depth(column 6, lines 25-50) fig. 3b; forming an insulating sidewall (44) on a side surface of the gate electrode (36) while restoring a crystal structure of the amorphous layer in a region from the first depth(40) to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth (column 7, lines 56-67;column 8, lines 1-4), the restoration of the crystal structure of the amorphous layer

being caused by heat treatment of a prescribed temperature which is conducted during formation of the sidewall (column 7,lines 25-34; column 7, lines 55-67); after the heat treating, forming a first impurity layer (28) of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions on both sides of the gate electrode in the amorphous layer extending from the surface of the semiconductor region to the second depth (column 7, lines 15-23; column 8, lines 1-4); and restoring a crystal structure of the amorphous laver in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy (column 8, lines 1-4).

Regarding claim 16, En et al. discloses wherein the prescribed temperature is in a range of 475°C to 600°C (column 7, lines 56-67).

Regarding claim 24, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C (column 7, lines 55-67).

Regarding claim 25, En et al. discloses wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy (column 7, lines 15-23; column 8, lines 1-4).

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 5 & 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (US Patent 6,893,930 B1).

Regarding claim 5, Yu et al. ('930) discloses a method for manufacturing a semiconductor device, comprising the steps of: forming an amorphous layer (252/254) in a region from a surface of a semiconductor region of a first conductivity type (inherent to have the semiconductor region of a first conductivity type ; En et al. US Patent 6,548,361 B1 column 5, lines 30-35) to a first depth (column 9, lines 30-42) fig. 19 ; by heat treating the amorphous layer at a prescribed temperature (column 9, lines 43-55), restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth (Examiner notes that the recitation "restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth" simply expresses the intended result of the process step positively recited *Minton v. Nat's Ass'n of Securitites Dealers, Inc.,* 336 F.3d 1373, 1381, 67 USPQ2d 1614, 1620 (Fed. Cir. 2003); See also MPEP § 2111.04.); after the heat treating, forming a first impurity layer (Sb)of a second conductivity type which has a pn junction (262/264) at a third depth that is shallower than the second depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth (column 9, lines 62-67; column 10, lines 1-9) ; and restoring a crystal structure of the

amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy (column 10, lies 10-20; lines 30-34).

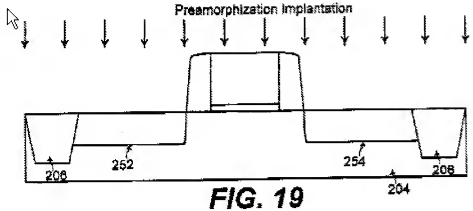

FIG. 19

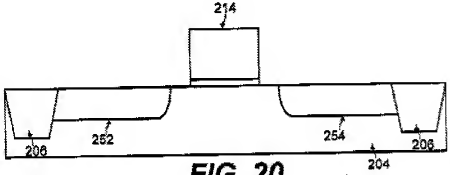

FIG. 20

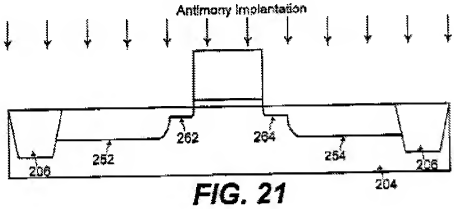

FIG. 21

Regarding claim 18, Yu et al. ('930) discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C (column 10, lines 10-20).

Regarding claim 19, Yu et al. ('930) discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 700 °C (column 10, lines 10-20).

Regarding claim 20, Yu et al. ('930) discloses wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy (column 10, lines 10-20).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over En (US Patent 6,548,361 B1) in view of Yu (US Patent 6,893,930 B1).

Regarding claim 6, En et al. discloses all the claim limitations of claim 5 except for wherein the third depth is range of 5 nm to 15 nm.

However, Yu et al. ('930) discloses wherein the third depth is lower than about 200 Å (20 nm) (column 10, lines 1-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made such that the third depth is in a range

of 5 nm to 15 nm since where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

11. Claims 6 & 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US Patent 6,893,930 B1).

Regarding claim 6, Yu et al. ('930) discloses all the claim limitations of claim 5 and further teaches wherein the third depth is lower than about 200 Å (20 nm) (column 10, lines 1-10) except for in a range of 5 nm to 15 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made such that the third depth is in a range of 5 nm to 15 nm since where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

Regarding claim 7, Yu et al. ('930) discloses wherein the prescribed temperature is in a range of 500°C to 650°C (column 9, lines 43-53) except for in a range of 475°C to 600°C, It would have been obvious to one of ordinary skill in the art at the time the invention was made such that the prescribed temperature is in a range of 475°C to 600°C since where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over En (US Patent 6,548,361 B1) in view of Yu (US Patent 6,521,502 B1).

Regarding claim 14, En et al. discloses all the claim limitations of claim 13 except for after the step of forming the first impurity layer, forming a second impurity layer of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer.

However, Yu et al. ('502) teaches after the step of forming the first impurity layer 20 & 22 (40 & 42), forming a second impurity layer 50 & 52 of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer (fig. 4; column 6, lines 8-14 & 16-18). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of En et al. with the of Yu et al. ('502) since doing so would form steep junctions, which is desirable for transistors with small dimensions.

13. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over En (US Patent 6,548,361 B1) in view of Yu (US Patent 6,893,930 B1).

Regarding claim 15, En et al. discloses all the claim limitations of claim 13 except for wherein the third depth is range of 5 nm to 15 nm.

However, Yu et al. ('930) discloses wherein the third depth is lower than about 200 Å (20 nm) (column 10, lines 1-10). It would have been obvious to one of ordinary

skill in the art at the time the invention was made such that the third depth is in a range of 5 nm to 15 nm since where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

14. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu En (US Patent 6,548,361 B1) in view of Wu (US Patent 6,391,751).

Regarding claim 17, En et al. discloses all the claim limitations of claim 13 but fails to teach that the gate electrode is formed is non-uniformly formed distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. Ia & Ib; column 1, lines 51-52). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of En et al. with the gate electrode formed non-uniformly on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

15. Claims 9, 11, & 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over En (US Patent 6,548,361 B1) in view of Yu (US Patent 6,521,502 B1).

Regarding claim 9, En et al. discloses a method for manufacturing a semiconductor device, comprising the steps of: forming a gate electrode (36) on a semiconductor region of a first conductivity type with a gate insulating film(38/56) interposed there between(column 5, lines 30-35;column 6, lines 14-24); forming an amorphous layer (64) in a region from a surface of the semiconductor region-to a first depth(column 6, lines 25-50); by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth(column 7, lines 56-67;column 8, lines 1-4); after the heat treating, forming a first impurity layer (28) of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth(column 7, lines 15-23; column 8, lines 1-4); after the heat treating, forming a second impurity layer (30) of a first conductivity type which has a pn junction by introducing ions into the heat treated amorphous layer(column 7, lines 35-55; column 8, lines 1-4); and restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy (column 8, lines 1-4)except for at a level that is shallower than the first depth and deeper than the third depth.

However, Yu et al. ('502) teaches forming a second impurity layer (50/52) at a level that is shallower than the first depth and deeper than the third depth(fig. 4; column 6, lines 8-14 & 16-18). Since En et al. teaches that one skilled in the art will appreciate,

the amorphizing implant, the offset spacers 42, the extension 28 implantation, the sidewall spacers 44 and the deep implants 30 can all be controlled (e.g., in terms of lateral width for the spacers 42 and 44 and in term of species type, dose and energy for the implantations) to arrive at the desired configuration of the damaged regions 40 and the anneal cycle can be controlled to regulate the amount of residual damage left by the amorphous areas 64.It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of En et al. with forming a second impurity layer (50/52) at a level that is shallower than the first depth and deeper than the third depth as taught by Yu et al. ('502) since doing so would form steep junctions, which is desirable for transistors with small dimensions and further would have been a matter of design choice of the semiconductor device.

Regarding claim 11, En et al. discloses wherein the prescribed temperature is in a range of 475°C to 600°C (column 7, lines 56-67).

Regarding claim 21, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C(column 7, lines 56-67).

Regarding claim 22, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 700 °C(column 7, lines 56-67).

Regarding claim 23, En et al. discloses wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy (column 8, lines 1-4).

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over En (US Patent 6,548,361 B1) in view of Yu (US Patent 6,521,502 B1) as applied to claim 9 and further in view of Yu (US Patent 6,893,930 B1).

Regarding claim 10, En et al. as modified by Yu et al ('502) discloses all the claim limitations of claim 9 except for wherein the third depth is range of 5 nm to 15 nm.

However, Yu et al. ('930) discloses wherein the third depth is lower than about 200 Å (20 nm) (column 10, lines 1-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of En et al. & Yu et al. ('502) with the teachings of Yu et al ('930) such that the third depth is in a range of 5 nm to 15 nm since where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over En (US Patent 6,548,361 B1) in view of Yu (US Patent 6,521,502 B1) as applied to claim 9 and further in view of (US Patent 6,391,751).

Regarding claim 12, En et al. as modified by Yu et al. ('502) discloses all the claim limitations of claim 9 but fails to teach that the gate electrode is formed is non-uniformly formed distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. Ia & Ib; column 1, lines 51-52). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of En et al. & Yu et al. ('502) with the gate electrode formed non-uniformly on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

18. Claims 5-7 & 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of En (US Patent 6,548,361 B1).

Regarding claim 5, AAPA discloses a method for manufacturing a semiconductor device, comprising the steps of: forming an amorphous layer (13) in a region from a surface of a semiconductor region of a first conductivity type to a first depth; by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer (shrinks to the second depth; forming a first impurity layer (15) of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth fig. 6(a)-7(b) [0007-0015] except for form a first impurity layer after the heat treating. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a first impurity layer after the heat treating since the selection of any order of performing process steps is prima facie obvious in the absence

of new or unexpected results; In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) The Admitted Prior Art further fails to teach restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy except for the order of after the heat treating forming a first impurity layer.

However, En et al. discloses restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy (column 7, lines 15-23; column 8, lines 1-4). Furthermore, En et al. discloses heat treating after forming a first impurity layer by way of performing separate anneal cycles to activate dopant species and recrystalize amorphous regions (column 8, lines 1-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the AAPA with the teachings of En et al. since doing so would recrystalize and activate the dopant species.

Regarding claim 6, AAPA discloses wherein the third depth is in a range of 5 nm to 15 nm [0015].

Regarding claim 7, AAPA discloses wherein the prescribed temperature is in a range of 475°C to 600°C [0012].

Regarding claim 18, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C (column 7, lines 56-67; column 8, lines 1-4).

Regarding claim 19, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 700 °C (column 7, lines 56-67; column 8, lines 1-4).

Regarding claim 20, En et al. discloses wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy (column 8, lines 1-4).

19. Claims 9-11 & 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA)) in view of En (US Patent 6,548,361 B1).

Regarding claim 9, AAPA discloses a method for manufacturing a semiconductor device, comprising the steps of: forming a gate electrode (12) on a semiconductor region of a first conductivity type with a gate insulating film(11) interposed there between; forming an amorphous layer (13)in a region from a surface of the semiconductor region to a first depth; by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth; forming a first impurity layer (15) of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth; forming a second impurity layer of a first conductivity type (16) which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions into the heat-

treated amorphous layer except for forming a first impurity layer and second impurity layer after the heat treating. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a first impurity layer and second impurity layer after the heat treating since the selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results; In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) The Admitted Prior Art further fails to teach restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy except for the order of after the heat treating forming a first impurity layer.

However, En et al. discloses restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy (column 7, lines 15-23; column 8, lines 1-4). Furthermore, En et al. discloses heat treating after forming a first impurity layer and second impurity layer by way of performing separate anneal cycles to activate dopant species and recrystalize amorphous regions (column 8, lines 1-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the AAPA with the teachings of En et al. since doing so would recrystalize and activate the dopant species.

Regarding claim 10, AAPA discloses wherein the third depth is in a range of 5 nm to 15 nm [0015].

Regarding claim 11, AAPA discloses wherein the prescribed temperature is in a range of 475°C to 600°C [0012].

Regarding claim 21, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C (column 7, lines 56-67; column 8, lines 1-4).

Regarding claim 22, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 700 °C (column 7, lines 56-67; column 8, lines 1-4).

Regarding claim 23 En et al. discloses wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy (column 7, lines 56-67;olumn 8, lines 1-4).

20. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of En (US Patent 6,548,361 B1) as applied to claim 9 and further in view of (US Patent 6,391,751).

Regarding claim 12, AAPA as modified by En et al. discloses all the claim limitations of claim 9 but fails to teach that the gate electrode is formed is non-uniformly formed distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. Ia & Ib; column 1, lines 51-52). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of AAPA & En et al. with the gate electrode formed non-uniformly

on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

21. Claims 13-16 & 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA)) in view of En (US Patent 6,548,361 B1).

Regarding claim 13, AAPA discloses a method for manufacturing a semiconductor device, comprising the steps of: forming a gate electrode (12) on a semiconductor region of a first conductivity type with a gate insulating film (11) interposed there between; forming an amorphous layer in a region from a surface of the semiconductor region to a first depth; forming an insulating sidewall (17) on a side surface of the gate electrode while restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth, the restoration of the crystal structure of the amorphous layer being caused by heat treatment of a prescribed temperature which is conducted during formation of the sidewall; forming a first impurity layer (15)of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions on both sides of the gate electrode in the amorphous layer extending from the surface of the semiconductor region to the second depth fig. 6(a)-7(b) [0007-0015] except for forming a first impurity layer after the heat treating. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a first impurity layer after the heat treating since the selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results; In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930)

The Admitted Prior Art further fails to teach restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy except for the order of after the heat treating forming a first impurity layer.

However, En et al. discloses restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy (column 7, lines 15-23; column 8, lines 1-4). Furthermore, En et al. discloses heat treating after forming a first impurity layer by way of performing separate anneal cycles to activate dopant species and recrystalize amorphous regions (column 8, lines 1-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the AAPA with the teachings of En et al. since doing so would recrystalize and activate the dopant species.

Regarding claim 14, AAPA discloses after the step of forming the first impurity layer (15), forming a second impurity layer (16) of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer fig. 6(a)-7(b) [0007-0015].

Regarding claim 15, AAPA discloses wherein the first impurity layer has a depth of 5 nm to 15 nm [0015].

Regarding claim 16, AAPA discloses wherein the prescribed temperature is in a range of 475°C to 600°C [0012].

Regarding claim 24, En et al. discloses wherein the step of restoring the crystal structure using solid phase epitaxy is conducted by heat treatment in a temperature range of 500 °C to 800 °C (column 7, lines 55-67).

Regarding claim 25, En et al. discloses wherein the first impurity layer is activated in the step of restoring the crystal structure using solid phase epitaxy (column 7, lines 15-23; column 8, lines 1-4).

22. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of En (US Patent 6,548,361 B1) as applied to claim 9 and further in view of (US Patent 6,391,751).

Regarding claim 17, AAPA as modified by En et al. discloses all the claim limitations of claim 13 but fails to teach that the gate electrode is formed is non-uniformly formed distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. Ia & Ib; column 1, lines 51-52). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of AAPA & En et al. with the gate electrode formed non-uniformly on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited for disclosing related limitations of the applicant's claimed and disclosed invention: Noda (US Pub no. 2004/0072394 A1); Borland (US Patent 6,187,643 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LATANYA CRAWFORD whose telephone number is (571)270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571)-272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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